

REMARKS

In response to the Office Action mailed October 6, 2003, Applicants amend their reissue patent application and request reconsideration in view of the amendment and following remarks. No claims are added or cancelled so that claims 1-18 remain pending.

The PTOL-326 Form accompanying the Office Action indicates recognition of a claim for the priority of a provisional U.S. patent application. There is no such priority claim. After the filing of the reissue patent application, the U.S. Patent and Trademark Office issued an incorrect filing receipt showing an incorrect serial number for the application that matured into a patent for which reissue is sought. The filing receipt showed the incorrect patent number as well. Additional domestic priority information appeared, based upon the patent incorrectly mentioned, including a claim of priority to a provisional U.S. patent application. Although a corrected filing receipt was requested, the correct filing receipt received was incorrect as to the priority claims. The domestic priority claim information, all of which was incorrect, continued to appear on the filing receipt and there was no indication of the claim of foreign priority. A second request for correction of the filing receipt has been filed. In the meantime, the Examiner should, if necessary, correct the Official Records to indicate that there is no claim of domestic priority to a provisional patent application and to show the foreign priority claim.

The Declaration was declared defective because it lacked the statement that the inventors were not only the original, but also the first inventors. This requirement appears in 37 CFR 1.63(a)(4), which was not cited with respect to this defect. In response to the assertion that Declaration was defective, a substitute Declaration is supplied. The Examiner also stated that the Declaration must state that the inventor is the "sole" inventor pursuant to 37 CFR 1.63(a)(4). It is believed that the Examiner intended to refer to 37 CFR 1.63(b)(2) which pertains to a statement that the inventors have read and understood the claims as well as the amendments submitted with the reissue application. The substitute Declaration responds to the ground that it is believed the Examiner intended to cite in asserting that the Declaration was defective. It would be incorrect to refer to a sole inventor here when four inventors are identified in the issued patent.

The Examiner stated that "no statement pursuant to 37 CFR 3.73(b)" has been received. This statement is incorrect. Pursuant to 37 CFR 3.73, the establishment of ownership "may be combined with the paper that requests or takes the action". Here, the statement pursuant to 37 CFR 3.73 was combined with and made part of the document titled "Assent of Assignee and Offer to Surrender". The Examiner's attention is directed to the next to the last paragraph of that

document which includes the required statement citing the basis for the assertion of title, referring to an assignment recorded in the U.S. Patent and Trademark Office. This statement entirely meets the requirements of 37 CFR 3.73(b), invoking subsections (1) and (ii). Acknowledgement of the receipt of this statement, fulfilling the requirement, in the next communication is respectfully requested.

The Examiner pointed out the necessity of returning the original Letters Patent before allowance of this reissue patent application. The original Letters Patent will be returned upon satisfactory prosecution of the present patent application, pursuant to the Offer to Surrender filed with this reissue patent application.

The amendments to the claims here are identical to the amendments in the Preliminary Amendment filed with the patent application with the following exceptions. In this Amendment, a comma is added in the final paragraphs of each of claims 1, 2, and 3, original claims of the issued patent. In the first newly added claim, claim 10, an error in the final paragraph is corrected. The reference in the first line of that paragraph to a random access memory with a command decode system duplicates the first line of the previous paragraph of that claim and is an obvious error. When claim 10 is compared to claim 1 of the issued patent, it is apparent that reference to a control circuit was intended in the first line of the final paragraph of claim 10. As intended, amended claim 10, in the final paragraph, now refers to a random access memory control circuit.

Newly added claims 10-18 were rejected as including new matter, asserting that the term "random access memory" is not supported by the disclosure of the patent that is sought to be reissued. Applicants traverse this rejection. Attention is directed to the original patent at column 13, lines 62-65. That paragraph points out that while the invention is described, for purposes of example, with respect to a synchronous dynamic random access memory (SDRAM), the invention can be applied to other types of RAMs that incorporate command decode systems. This passage, although brief, clearly supports the newly added claims 10-18.

Claims 2-6 were indicated as allowable if rewritten in independent form and claims 7-9 were allowed. No further comment on these original claims is necessary.

Claim 1 was rejected as obvious over Hwang et al. (U.S. Patent 5,901,304, hereinafter Hwang).

As an initial matter, if the Examiner intends to make this rejection of record, then a supplemental PTO-892 Form needs to be issued and entered in the file of this patent application. Hwang was not included with the Office Action and not identified on the PTO-892 Form. In order to expedite prosecution, Applicants have obtained a copy of that patent.

The Examiner relied upon Figures 3A, 3B, and 5 of Hwang in rejecting claim 1, asserting that Hwang describes all of the elements of that claim with the exception of an embedded SDRAM, instead of an embedded DRAM. However, Hwang does not disclose all of the elements of claim 1, even excluding that acknowledged difference.

Several of these differences, which prevent establishment of *prima facie* obviousness of claim 1 based upon Hwang are pointed out here.

The arrangement shown in Figures 3A and 3B of Hwang include DRAM macros, 202A and 202B in Figure 3A and 212A-212D in Figure 3B. These DRAM macros, which may be considered as a unit, constitute asynchronous RAM. The interface conversion circuits, 201 of Figure 3A and 211 of Figure 3B, receive input signals for synchronous RAM and generate control signals for the asynchronous RAM, namely the DRAM macros. In other words, the asynchronous RAM constituted by the DRAM macros is controlled by input signals for synchronous RAM.

By contrast with this construction of Hwang, in the invention as defined by claim 1, a synchronous dynamic random access memory (SDRAM) control circuit directly generates control signals for synchronous RAM. There is no command conversion circuit, nor any need for such a command conversion circuit, that could be compared to the interface conversion circuits of Hwang. The input signals generated by the DRAM control circuit are not converted but are directly input to synchronous RAM, for example, the synchronous DRAM core 104 of the embodiment of Figure 1 of the present patent application. Since the invention does not require an interface conversion, or command decoding, it can achieve high-speed operation through the synchronous core unit of claim 1.

Further, in comparing Hwang to claim 1, the Examiner asserted that the buffer 401 of Figure 5 of Hwang is a logic circuit that is comparable to the logic circuit 102 illustrated in the embodiments of the issued patent and equivalent to the logic circuit of claim 1.

No one of skill in the art would assert that a buffer circuit is a logic circuit. By definition, a logic circuit executes a logical operation on a signal. By contrast, a buffer merely holds an input signal until an appropriate time, for example, by delaying an input signal through a series of gates, so that the output of the signal is synchronized with other events. A buffer does not, for example, execute any of the logical OR, AND, NOR, and NAND functions, examples of functions executed by logic circuits. To prove the common understanding of these terms, buffer circuit and logic circuit, and the fact that they are different, pages 108 and 501 of the IEEE Standard Dictionary of Electrical and Electronics Terms (1984) are attached.

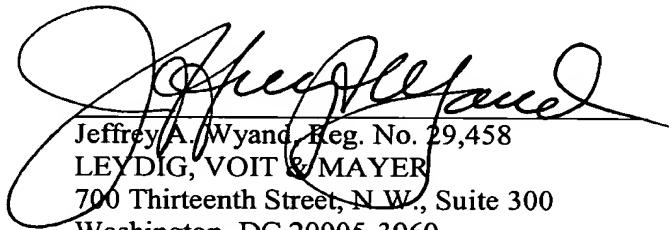
The assertion of equivalence between a buffer and a logic circuit is simply unsupported by common knowledge in the art and the disclosure of Hwang. Therefore, upon reconsideration,

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the rejection of claim 1 should be withdrawn and all of the original claims of the patent, claims 1-9, allowed. In addition, claims 10-18 should be allowed because, as already pointed out, those claims are supported by the original disclosure and parallel claims 1-9.

Reconsideration and allowance of all of claims 1-18 is appropriate and earnestly solicited.

Respectfully submitted,



Jeffrey A. Wyand, Reg. No. 29,458
LEYDIG, VOIT & MAYER
700 Thirteenth Street, N.W., Suite 300
Washington, DC 20005-3960
(202) 737-6770 (telephone)
(202) 737-6776 (facsimile)

Date: December 31, 2003
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